

Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1.-6. (Cancelled)

7. (Original) A method for producing a semiconductor laser device comprising the steps of:
forming a semiconductor multilayer structure on a semiconductor substrate of a first conductivity type, the semiconductor multilayer structure including: a cladding layer of the first conductivity type; an active layer having a super-lattice structure; a first cladding layer of a second conductivity type; an etching stop layer of the second conductivity type; a second cladding layer of the second conductivity type; a band graded layer of the second conductivity type; and an impurity supply control layer;

disordering the active layer by diffusing an impurity at least in a predetermined region within the semiconductor multilayer structure; and

patterning the second cladding layer into a ridge structure by wet etching,

wherein a concentration of the impurity diffused in the etching stop layer within the predetermined region is greater than a concentration of the impurity outside the predetermined region and equal to or smaller than about $2 \times 10^{18} \text{ cm}^{-3}$.

8. (Original) A method according to claim 7,

wherein the semiconductor substrate comprises a compound semiconductor material containing GaAs of the first conductivity type as a main component;

the cladding layer of the first conductivity type comprises a compound semiconductor material containing GaP of the first conductivity type as a main component;

the active layer comprises a compound semiconductor material containing GaP as a main component;

the first cladding layer, the etching stop layer, the second cladding layer, and the band graded layer each comprise a compound semiconductor material containing GaP of the second conductivity type as a main component; and

the impurity supply control layer comprises a compound semiconductor material containing GaAs as a main component.

9. (Original) A method according to claim 7,
wherein the semiconductor substrate comprises GaAs of the first conductivity type;
the cladding layer of the first conductivity type comprises AlGaInP of the first conductivity type;
the active layer includes a super-lattice structure comprising AlGaInP and GaInP;
the first cladding layer and the second cladding layer each comprise AlGaInP of the second conductivity type;
the etching stop layer comprises GaInP of the second conductivity type;
the band graded layer comprises GaInP of the second conductivity type; and
the impurity supply control layer comprises GaAs.
10. (Original) A method according to claim 7, wherein the impurity supply control layer has a thickness equal to or greater than about 100 Å.
11. (Original) A method according to claim 7,
wherein a concentration gradient of the impurity diffused in the second cladding layer within the predetermined region, taken along a normal direction to the substrate from an upper face toward a bottom face of the substrate, is greater than a concentration gradient of the impurity outside the predetermined region along the normal direction to the substrate, and is equal to or smaller than about $2 \times 10^{18} \text{ cm}^{-3} \mu\text{m}^{-1}$.
12. (Original) A method according to claim 7, wherein a concentration of the impurity diffused in the active layer within the predetermined region is greater than a concentration of the impurity outside the predetermined region, and is equal to or smaller than about $2 \times 10^{18} \text{ cm}^{-3}$.
13. (Original) A method according to claim 8, wherein the impurity is Zn.

Respectfully submitted,

Daniel N. Calder

Daniel N. Calder, Reg. No. 27,424
Attorney for Applicants

DNC/vj

Dated: November 3, 2003

<input checked="" type="checkbox"/> P.O. Box 980 Valley Forge, PA 19482 (610) 407-0700
<input type="checkbox"/> P.O. Box 1596 Wilmington, DE 19899 (302) 778-2600

The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express mail, with sufficient postage, in an envelope addressed to:
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

November 3, 2003

Kathleen L. Kelly

Express Mail No.: EV351885074US